MULTIPORT MEMORY WITH TWISTED BITLINES
ABSTRACT

Memory cell arrays are defined by rows and columns of memory cells that are addressed by sets of bitlines associated with a first memory port and a second memory port. The bitlines associated with the first memory port have bitline exchanges associated with a first set of memory cell rows and the bitlines associated with the second memory port have bitline exchanges associated with a second set of memory cell rows. The memory cells can have the same design, and all memory cell columns can have the same design. Read/write logic for the arrays can be based on memory cell row addresses.